Abstract Of The Disclosure

A method for monitoring a microprocessor and a circuit arrangement having a microprocessor are described. A microprocessor is monitored using an assigned watchdog. The watchdog monitors whether reset pulses are received within a time interval of predetermined duration. If the reset pulse is received, the time interval is reset and restarted. If reset pulses are not received, a reset of the microprocessor is initiated. In suitable operating phases of the microprocessor, a check function of the watchdog is activated. During the execution of the check function, first a reset of the watchdog is executed and then a sequence of waiting loops, whose duration is greater than the duration of the time interval of the watchdog, is executed.